Status of the CALICE Scintillator HCAL Engineering Prototype

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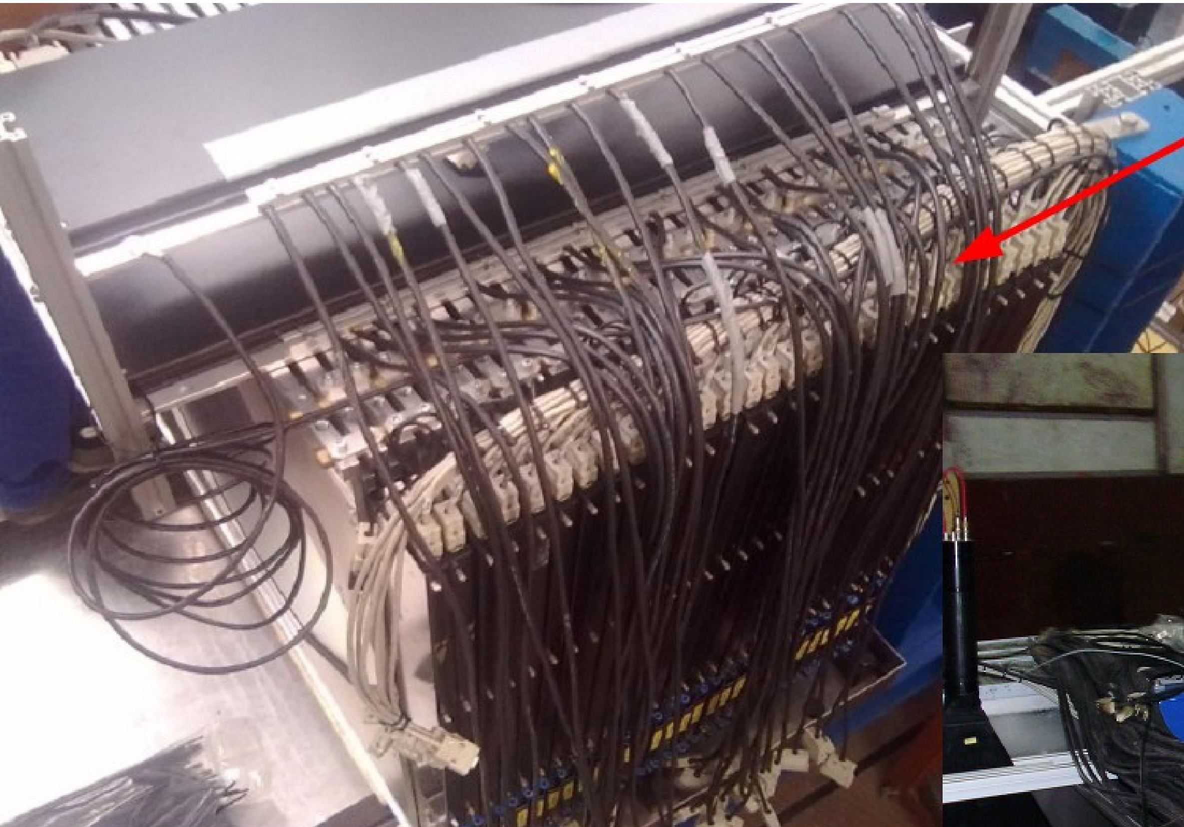
for the CALICE Collaboration
ECFA-LC 2013,
May 29th 2013

Overview

- AHCAL engineering prototype design and hardware
- LED calibration system update
- From single PCB to full prototype
  - Lab slab test
  - 2012 CERN layer
  - EM stack (and beyond)
- Other readout options
  - Tiles/SiPMs
  - HCAL/ECAL geometric options
- Conclusion/Outlook

AHCAL Physics Prototype

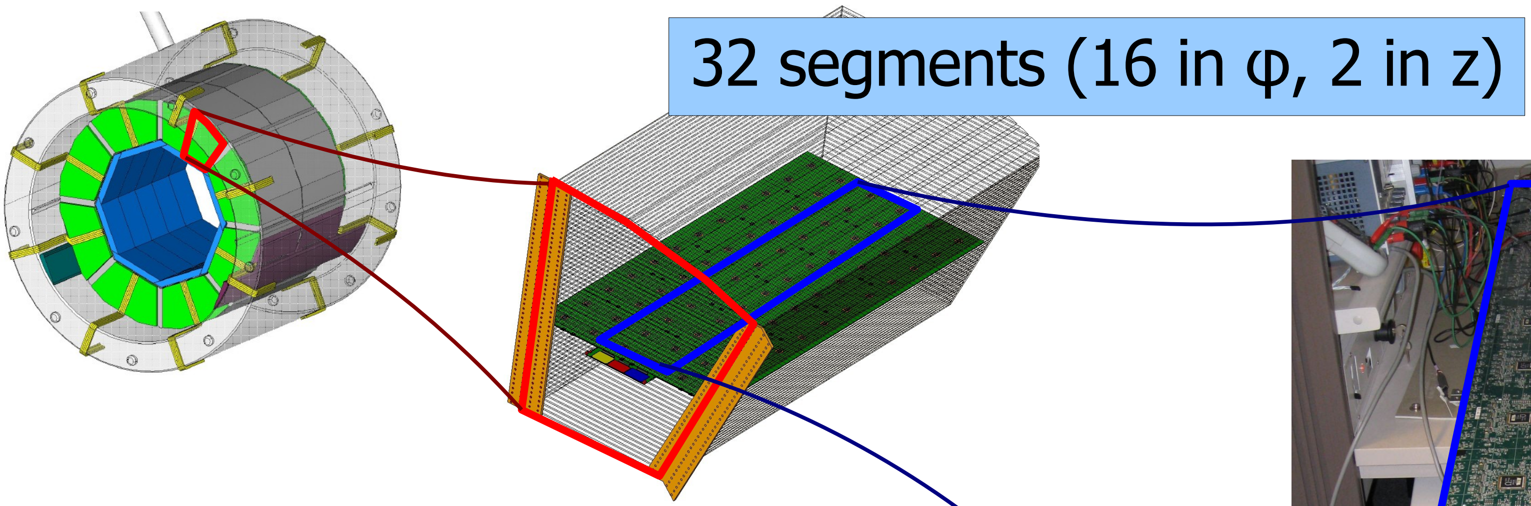


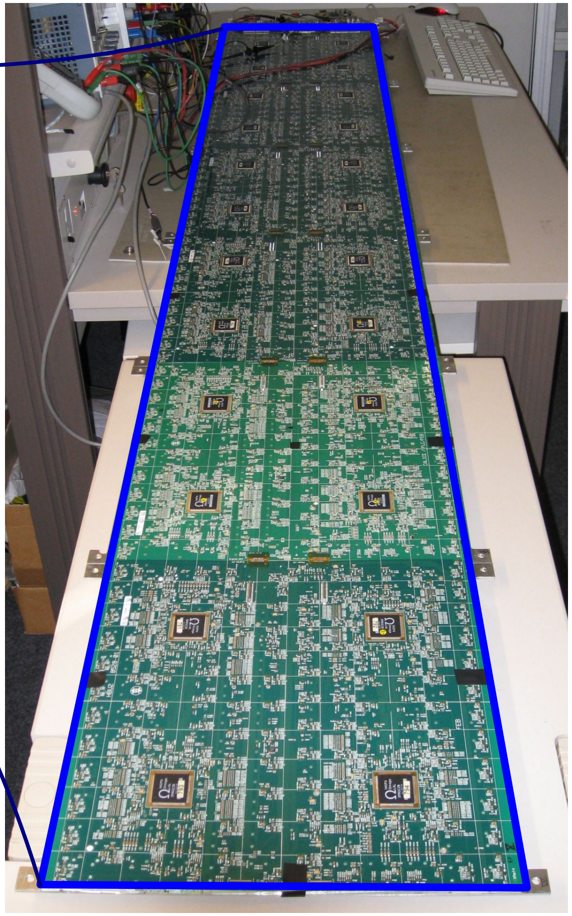
Cables for calibration boards

Cables from analog to digital part of electronics

Not scalable to full detector
→ Build realistic prototype

The AHCAL Engineering Prototype

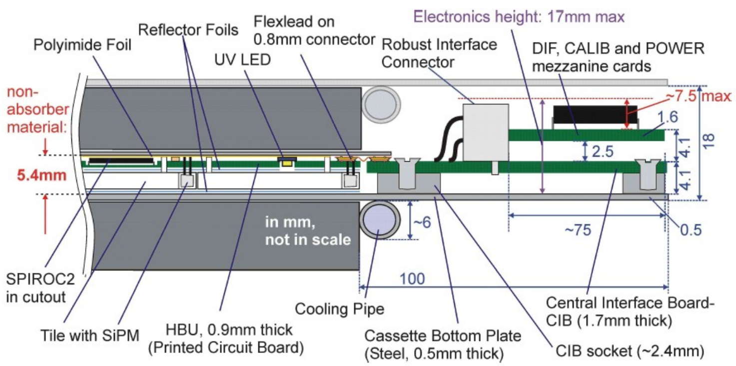




- 40 layers per half-octant
  - 3 *slabs* of 6 PCBs per layer
  - Millions of channels!
- Challenge: full electronics integration into layers
  - Readout, power, calibration etc.
  - Tight space between absorbers
  - No active cooling inside layers

Integrated electronics

- Layer built up of 18 HCAL Base Unit PCBs
  - extra thin PCBs (780um)
  - cutouts for ASICs
  - → only 5.4 mm thickness including 3mm tiles



- SPIROC2b: highly integrated ASIC for SiPM readout
  (developed by LLR, France)
  - Channel-wise bias adjustment
  - Channel-wise adjustable gain
  - ~1ns time stamping capability
  - Fully self triggered operation possible
  - Power pulsing → 25 µW/ch

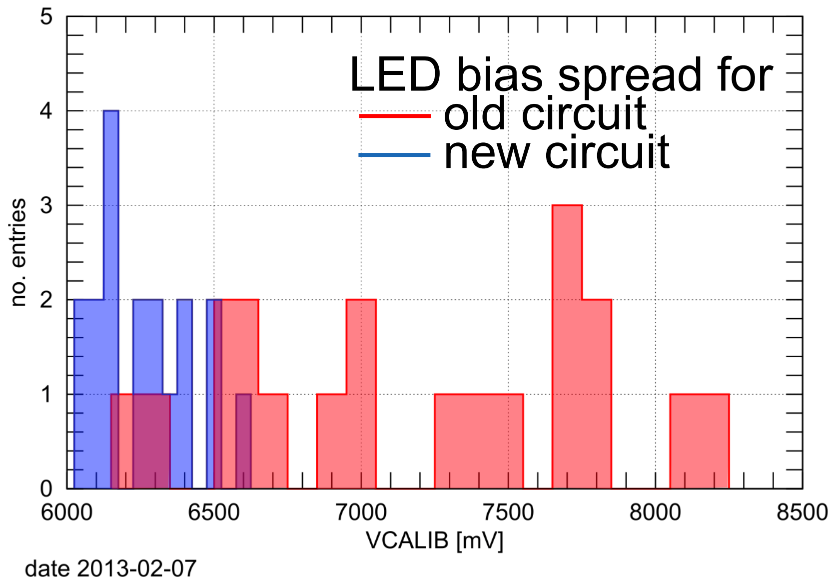
PCB cutout

LED Calibration System Update

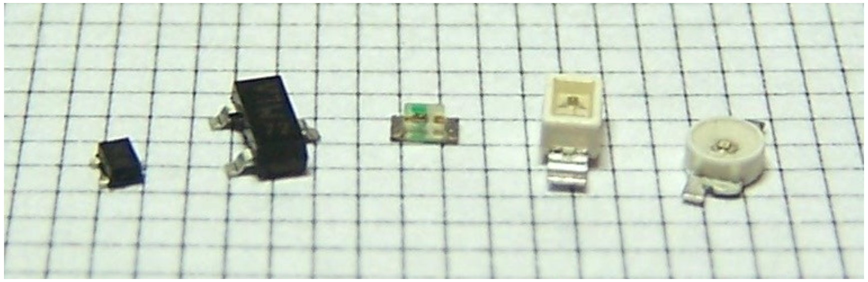
- Integrated calibration system for SiPM gain calibration (1 LED per channel)
- Showed some spread in LED amplitudes and timing
  - Small change in circuit layout

    → Now much more homogenous output

    → Substantially decreases calibration time



- Used LED type is discontinued
  - Uni Wuppertal is testing new LEDs
  - First candidate identified



The road to a full prototype

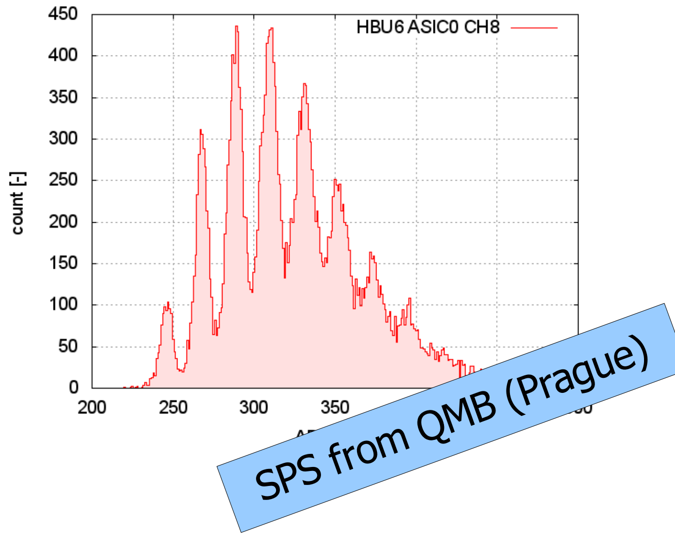
Operation modes to be tested:

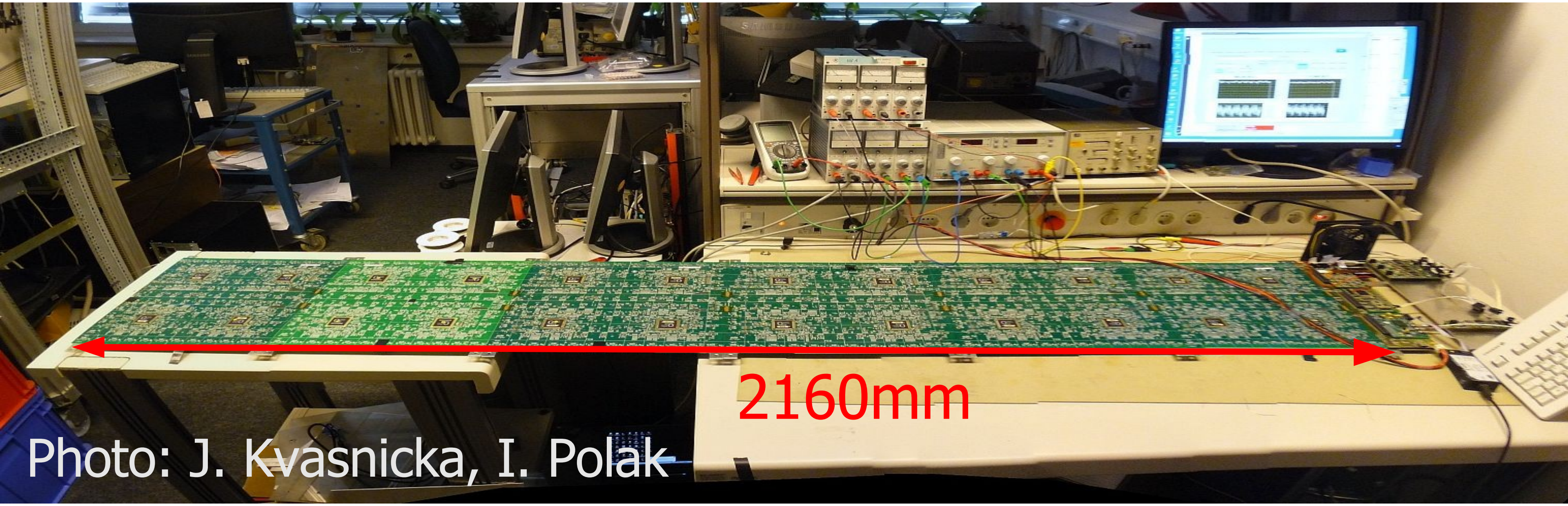
- Single boards in the lab ✓
- Single boards in testbeam ✓
- Multiple boards in one slab (1D extension)
- Multiple HBUs in one layer (2D extension)
- Multiple layers in one detector (3D extension)

Once operation is established, acquire more layers!

Full Slab Test

- Full slab assembled in lab
  - 6 serial HBUs
- Readout & calibration system tests (see talk by I. Polak in next session)
- Readout unhindered by 2.2m signal path
- 1D extension established





CERN Layer (2x2)

- 2012 CERN hadron beam
- 4 HBUs, 576 channels
- Fully autotriggered, low rates

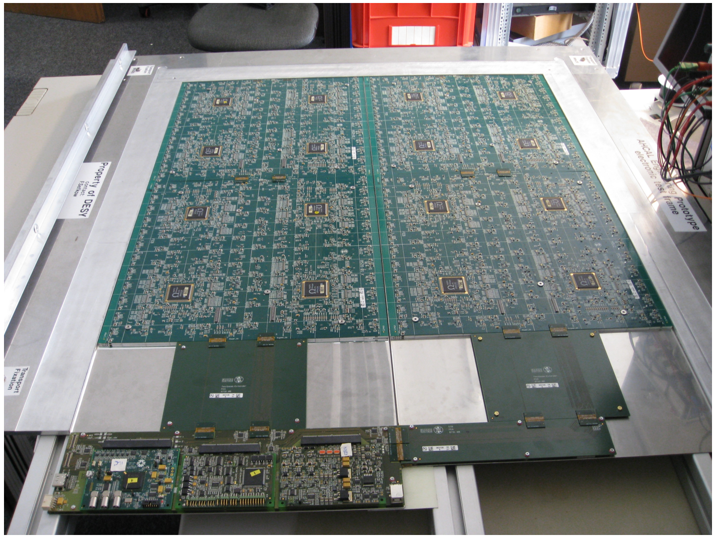
  → threshold setup very important
- Using common threshold is easiest:
  - Tile lightyield equalised by bias setup
  - SiPM gain equalised by preamplifier setup

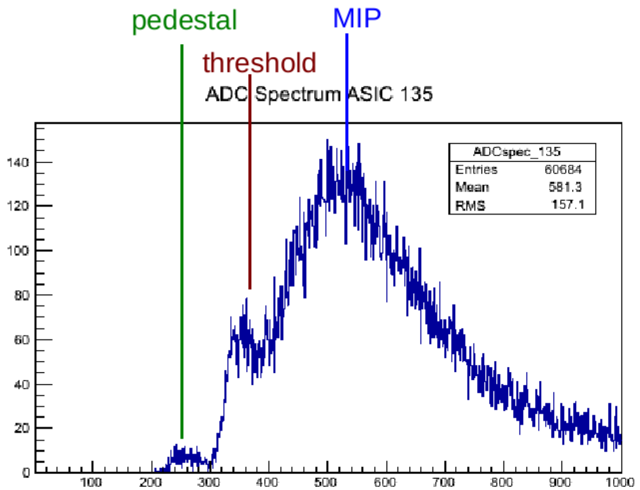
    → equalised MIP response

    → common threshold applicable
  - Worked out well

    → 2D extension established ✓

- See next talk by Shaojun Lu
  - Adding 1 time dimension



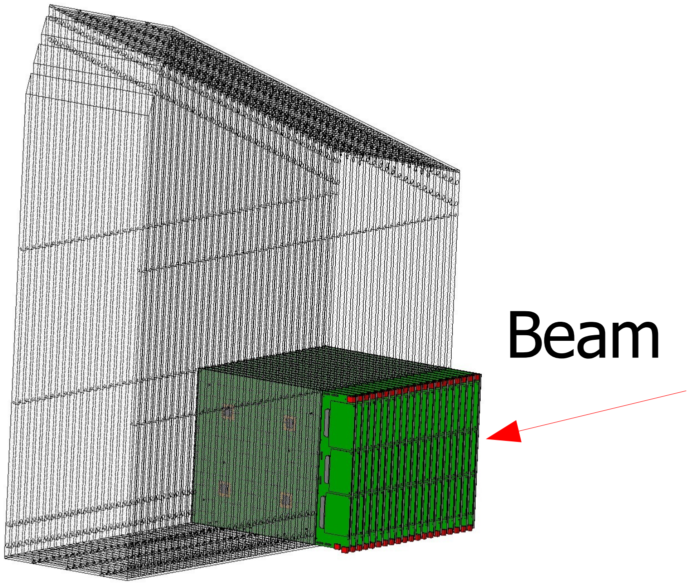


Towards a small HBU stack

- Intermediate goal: small stack for DESY electron beam
  - System tests, performance validation
  - Mechanics test
  - Flexible test bench for tile/SiPM options

- 4 HBUs available from CERN beam last year
  - 1 extra board commissioned from available tiles
  - 8 new PCBs available (Uni HH, DESY)

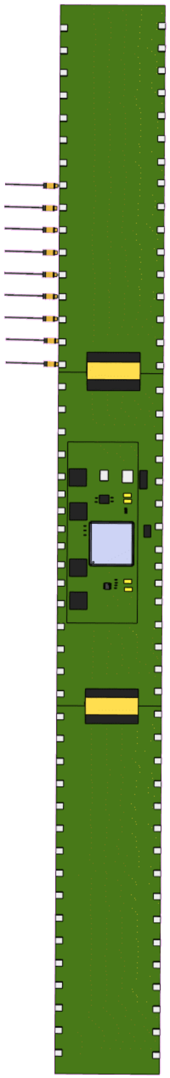
    → 5 HBUs usable right now,
    up to ~10 by end of year



- Air stack for cosmics/MIP calibration
- ILD absorber prototype (Fe) for EM showers

New DAQ System

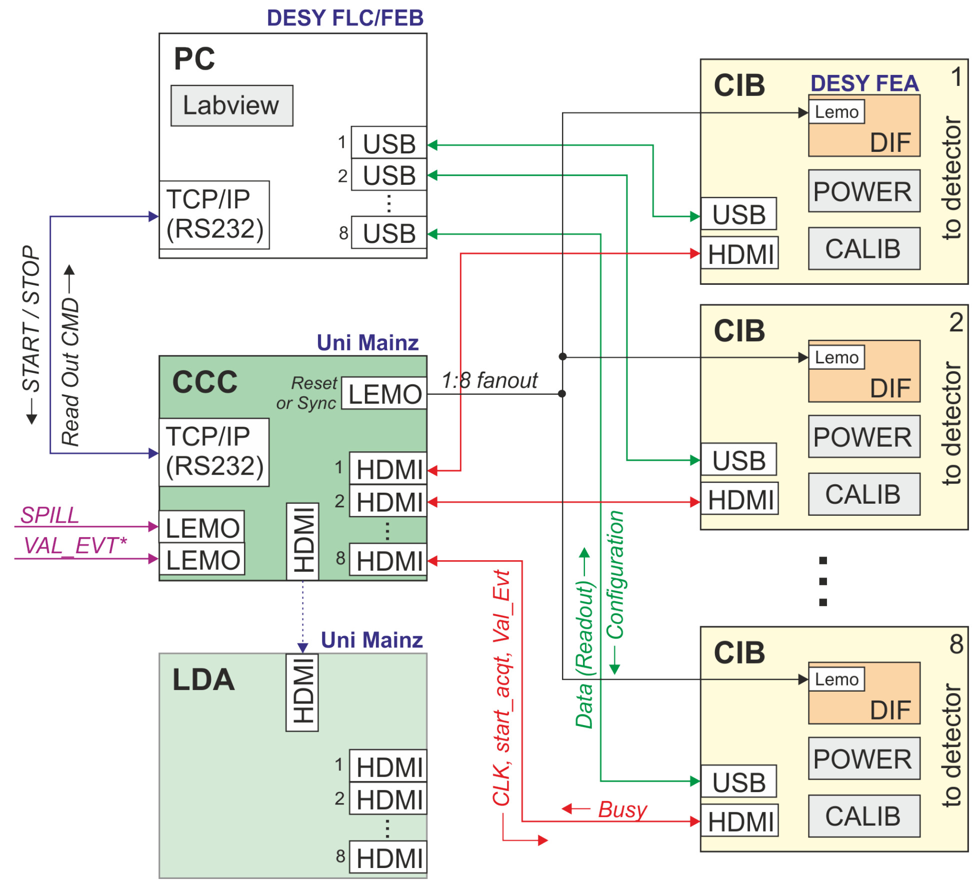
- DAQ used until this point not capable of synchronous multi-layer readout
- New developments based on redesigns of common CALICE DAQ hardware
  - DIF (NIU/Fermilab), new revision 2012
  - LDA, CCC (UK groups) redesigned by Uni Mainz
    - Based on new FPGA/SoC (Xilinx Zynq)
    - Now very flexible, powerful processing on board
    - Still compatible to CALICE DAQ
- Stepwise adaptation from USB data transfer to full HDMI
  - First stage: data via USB, fast signals (clock, triggers) via HDMI through CCC
  - White paper with development stages is available.
  - Conceptually close to CALICE DAQ designs
- Electronics & software 100% compatible to scintillator ECAL (Shinshu, Japan)



LDA: A. Welker (Mainz)

New DAQ System

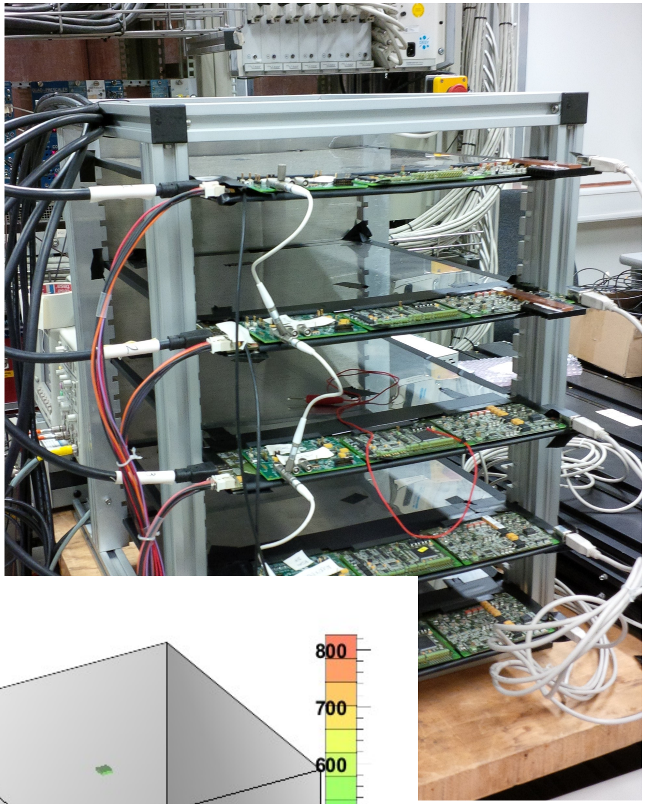
- First DAQ stage is implemented
- PC software still Labview based
  - 50% rewritten
  - Now fully multi threaded
    → True parallel readout
- Data readout completely functional
- Very stable operation (72h+ runs)
- Faster than ever (~factor 7)
- Next step: establish parallel data path through LDA for testing



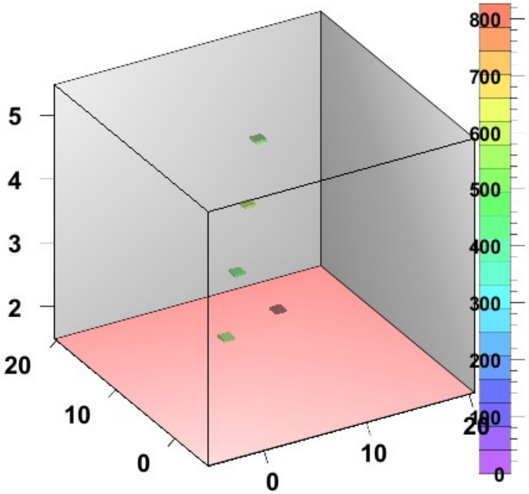
Cosmics stack

- Air stack for cosmic muons
  - External trigger validation by coincident scintillator paddles
  - Running on only 4 boards
  - First test with real particles
  - Very low rates (underground lab)

    → challenging threshold setup



- Long runs (whole weekends)
- No DAQ crashes
  - Software stability proven

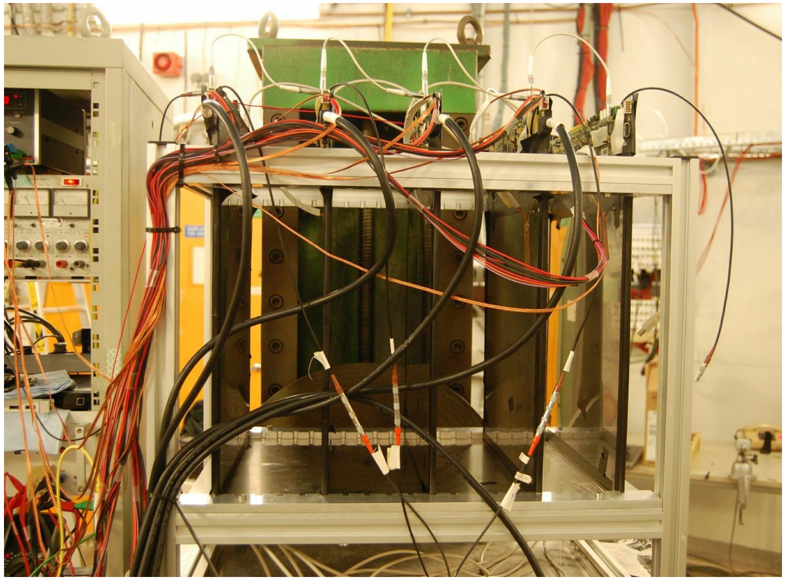


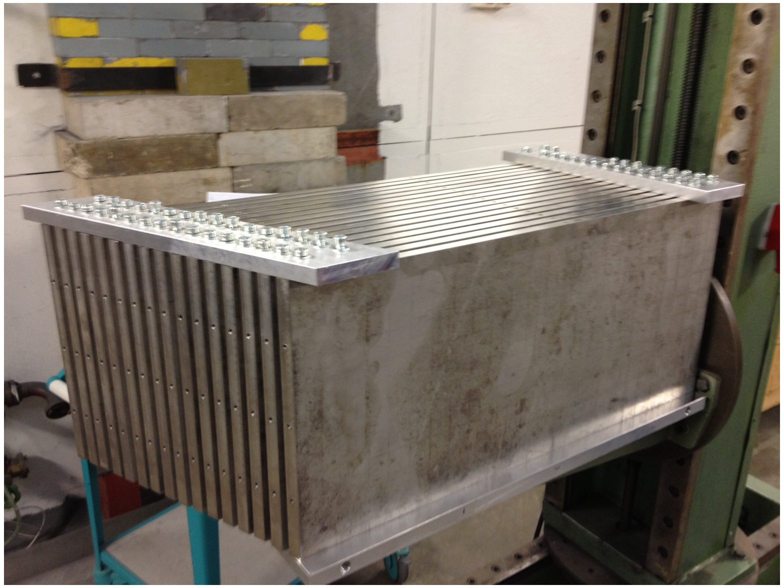
DESY Testbeam

- MIP calibration in air stack
  - 3GeV e^+
  - Crosscheck previous MIP calibration
  - New layer uncalibrated yet

- Energy scans in Fe stack
  - Capture some EM showers
  - First calorimetric results from HBUs

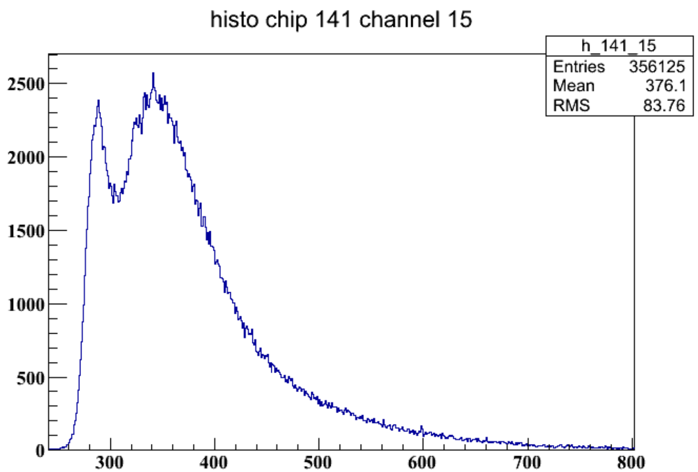
- Achievable resolution is limited by only 5 layers
  - Can add more layers as they come
  - Electronics available for 12 layers

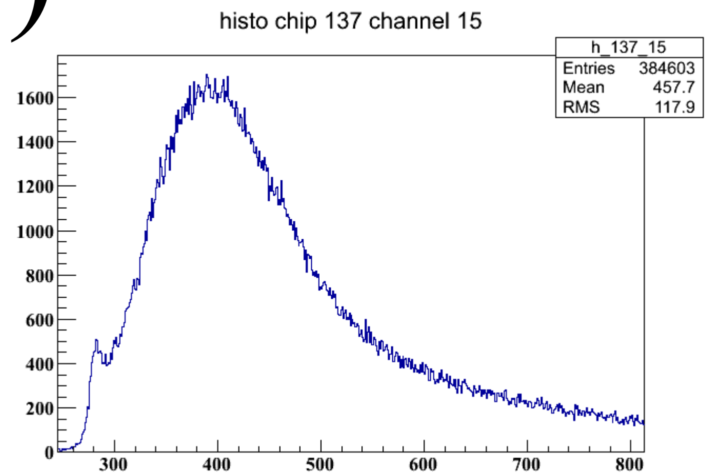


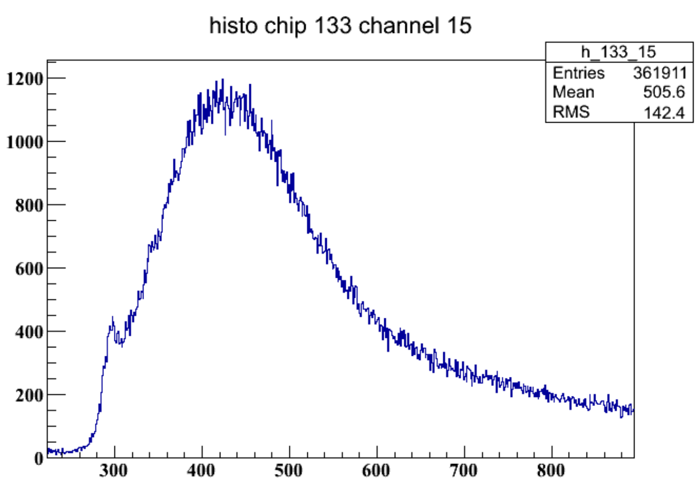


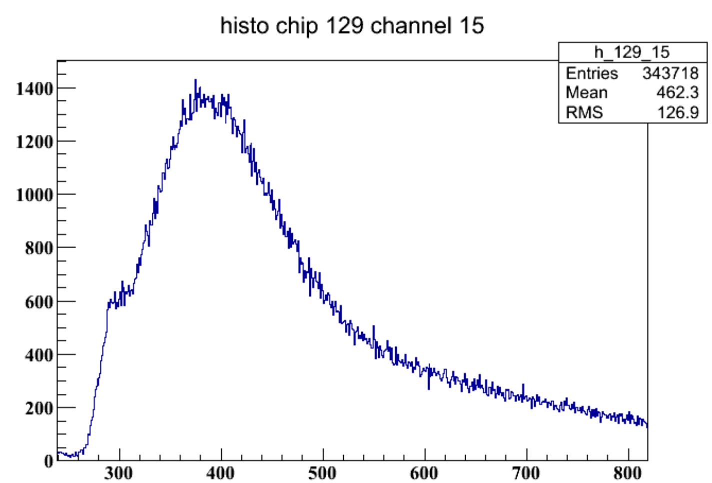
DESY testbeam results

- Synchronous MIP calibration through several layers
- 3D extension readout established (✓)









Flexible electronics

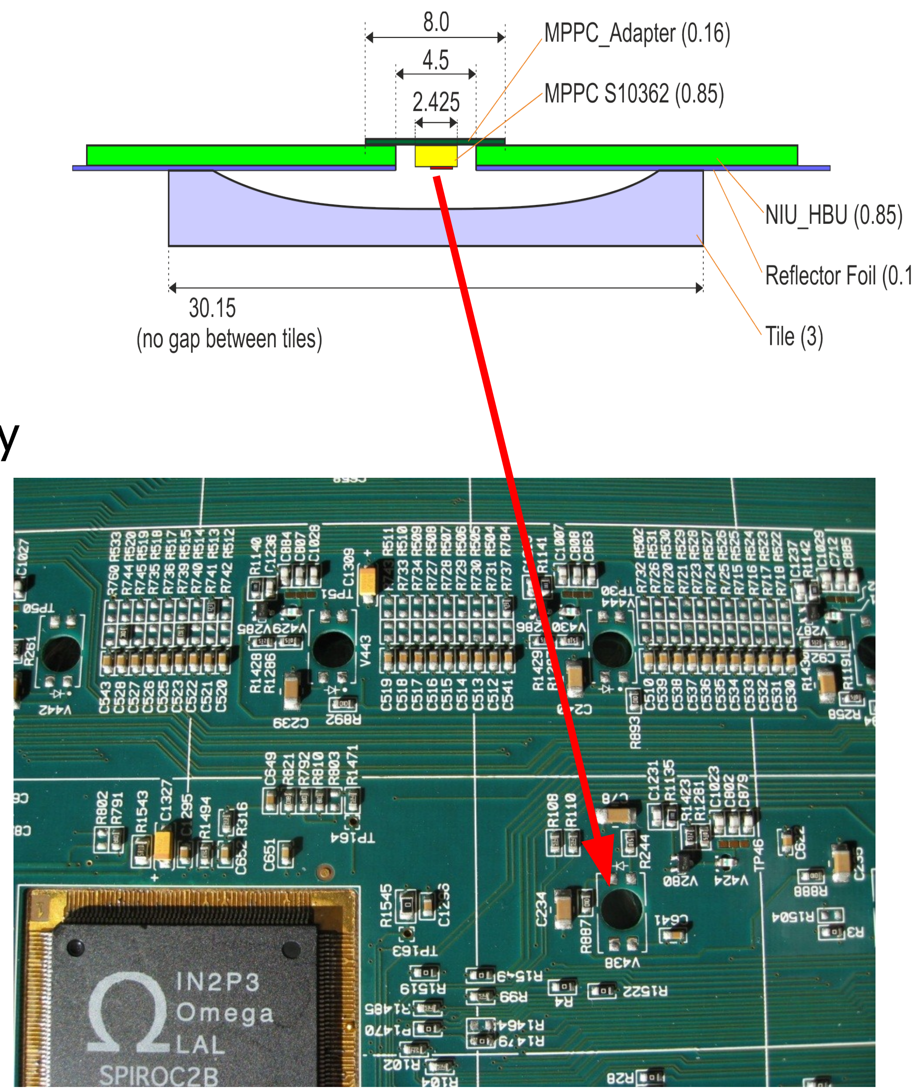
- AHCAL electronics are designed for operation in a full-scale collider detector
- ...but up to now, many parameters are not fully finalized
  - SiPM placement (side or top of tile)
  - Tile design (WLS vs. direct coupling)
  - SiPM type
  - Geometry (tile/strip)

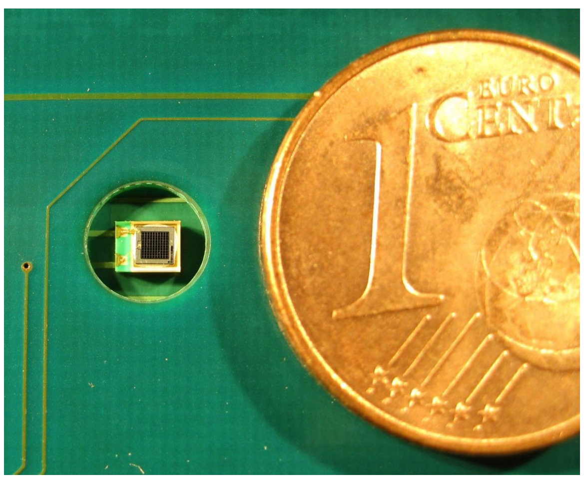
- Electronics are very flexible!

  → Proceed with integration and sensor optimisation in parallel

Surface mount HBU

- Mount SiPM on PCB, not in the tile
  (G. Blazey et al., NIM A605 (2009) 277,
  F. Abu-Ajamieh et al. NIM A659 (2011) 348)
- No gap between tiles
  - One “megatile” per HBU
- Concave cavity in tiles improves uniformity
- 2 surface mount HBUs produced
  - To be equipped with tiles

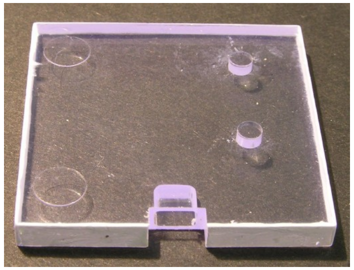




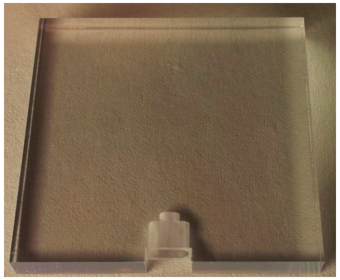
Direct coupling tiles

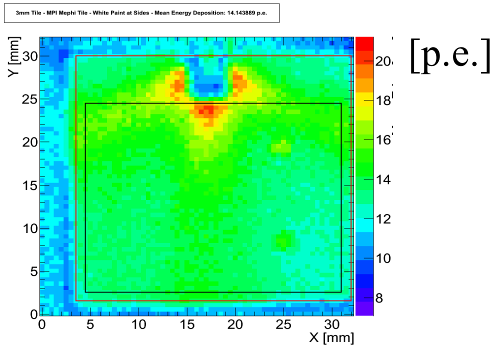
- WLS fibre has two tasks:
  - shift wavelength to sensitive range of SiPM
  - improve light yield uniformity within a tile
- new SiPMs are sensitive in blue-UV range
- optimised tile design allows good uniformity without WLS

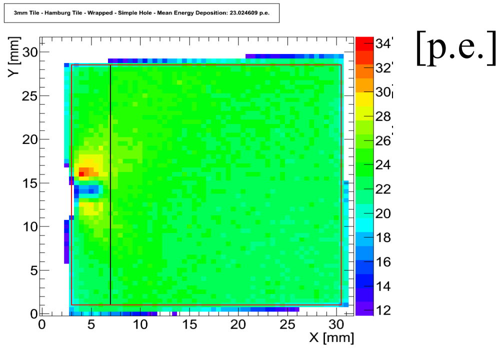
ITEP



Uni Hamburg



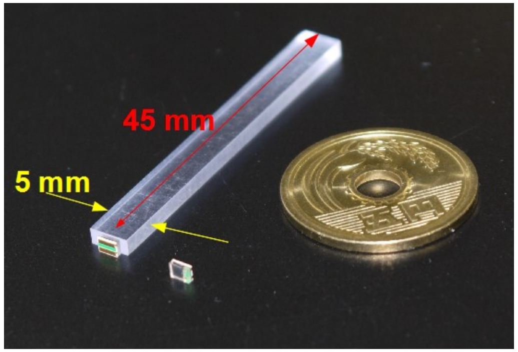




- Two different types:
  - ITEP: injection moulding, easily producible in large quantities
  - Uni Hamburg: machining
- Good uniformity of both types
  - Uni Hamburg type slightly better

Other Geometries: Strip Scintillator ECAL

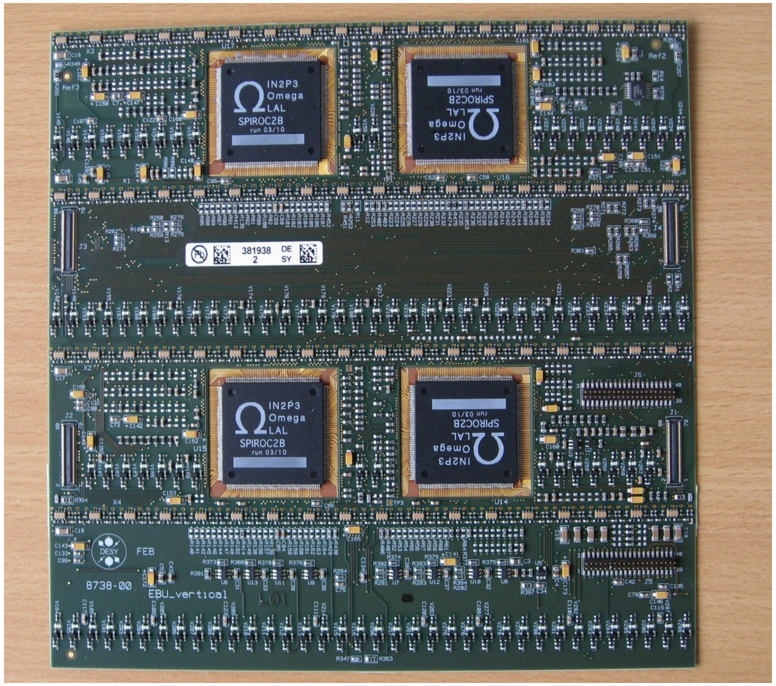
- ECAL option: needs finer granularity than HCAL
  - 45 * 5 mm² strips instead of 30 * 30 mm² tiles
  - 4 times larger channel density than HCAL
  - Alternating orientation horizontal / vertical

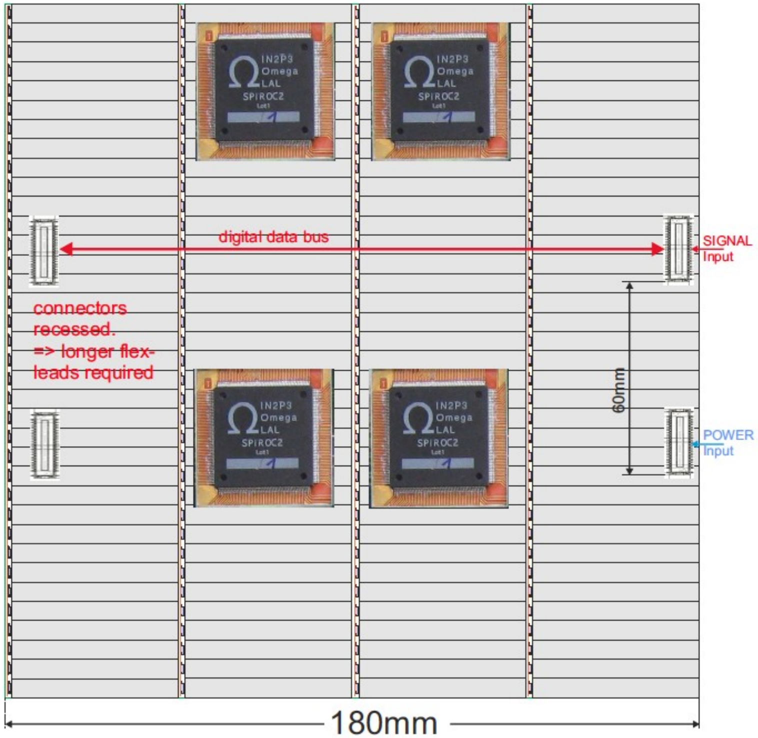


- SciECAL uses Hamamatsu MPPCs as SiPMs
  - 1600 pixels on 1 * 1 mm²
  - Gain: a few 10^5
  - Bias voltage ~70 V

EBU

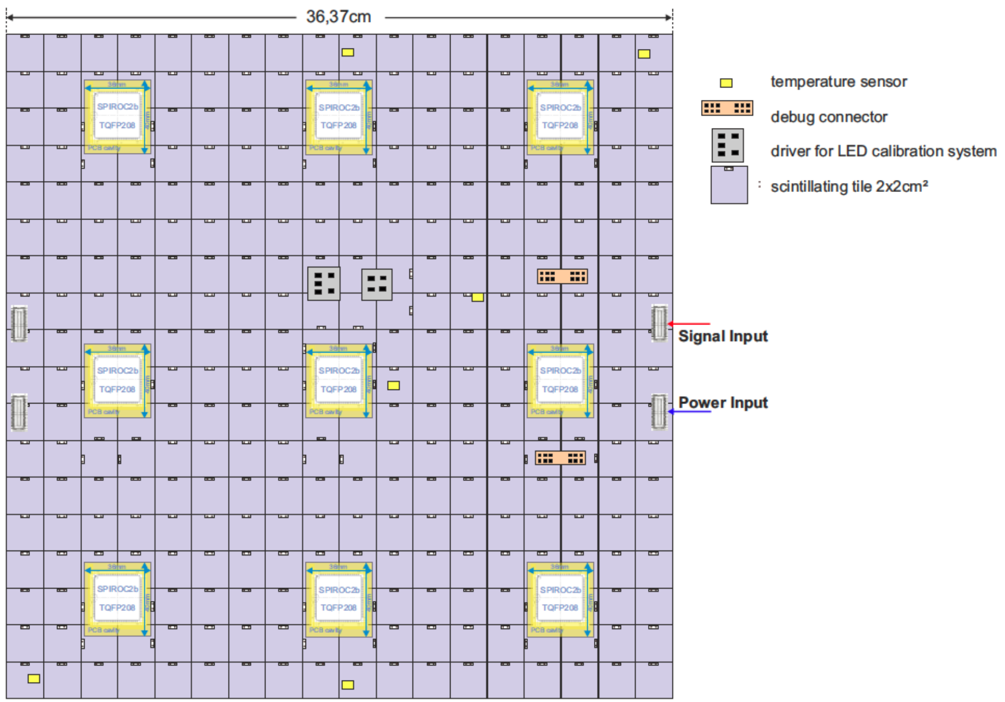
- HBU design scaled down to Scintillator strip ECAL dimensions
- Two PCB designs needed for different orientations
  - Vertical orientation already produced and tested
  - Horizontal orientation in design, needs minor changes in connectors

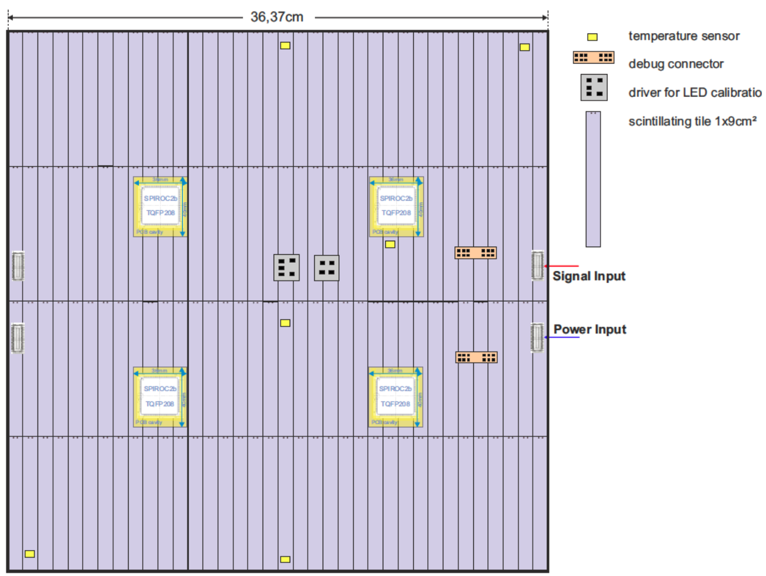


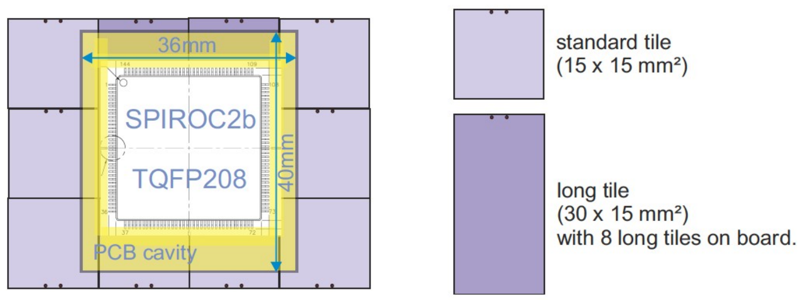


ECAL & HCAL geometries

- Different geometry PCBs also supported and explored
  - EBU: 20*20mm tiles
  - EBU: 15*15mm tiles
  - HBU: 90*10mm strips







Summary and Outlook

Summary

- Very versatile electronics provide effective testbench for different tile/SiPM concepts
- Multilayer DAQ based on CALICE DAQ hardware
  - Fast, stable operation so far
- First HBU stack setup commissioned
  - Small scale system test

Outlook

- Testbeam with 5+ layers ongoing
  - More layers to be added during the year → parasitic data taking
- Next step in DAQ development
  - Full HDMI readout
- Plan to be prepared once hadron beams return in 2014