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Dual readout—strip/pixel systems

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ABSTRACT

3D-electrode pixel detectors are proposed in which the bias electrodes are connected to form a strip readout on the same or opposite side of the sensor. It can provide a fast trigger and significantly increase spatial resolution in both directions. This combination is also possible with double-sided processing in planar technology. A second paper ("Dual Readout—3D Direct/Induced-Signals Pixel Systems") will cover another means of increasing spatial resolution without duplicating the complex pixel electronics.

1. Introduction

Pixel detector systems often have limited spatial resolution due to the necessary complexity of the readout electronics in each individual pixel, which then sets a lower limit on pixel area. In 3D silicon sensors [1–14], both electrode types are accessible from the front and backside of the wafer, and they can be joined by conductors in a number of different ways. High-resistivity polycrystalline silicon resistors can be fabricated on the sensor using standard technology and adding less than a micron of material. Capacitative readout has long been standard on double-sided silicon strip sensors and combined with polycrystalline silicon resistors in the bias-voltage supply lines, could be used here as well. Both pixel and micro-strip readouts with either polarity are possible. 3D sensors with strip readout and 3D sensors with pixel readout have both been successfully fabricated, and separately tested with LHC readout electronics.

In this paper we list several of the possible ways this combined technology could improve the performance of pixel detector systems. These will generally require extra fabrication steps and so are not recommended until high yields have been achieved in standard 3D fabrication steps. A second paper ("Dual Readout—3D Direct/Induced-Signals Pixel Systems") will cover another means of increasing spatial resolution without duplicating the complex pixel electronics. High-resolution pixel sensors have been fabricated, in one case with sub-μm spatial resolution, but without a complex readout circuit [15,16]. An example of spatial resolution obtained with typical microstrip readout systems compared with the more typical pixel dimensions of $100 \times 200\,\mu m^2$ is shown in Fig. 1 [17]. The pixel electrodes for this test were tied together and connected to a strip-readout chip for a beam test. The horizontal plot axis shows the y position at the pixel sensor plane predicted by a $4-y/2-x$ plane, 50 μm pitch, silicon strip detector system with $\pm 4\,\mu m$ accuracy for y at the pixel planes. The vertical plot axis shows the same y position reconstructed from the 200 μm-pitch signal electrodes of one of the 3D detectors under test. The 200 μm vertical steps visible in the plot separate points from tracks in adjacent pixels. The sharpness of the steps is a consequence of the telescope accuracy

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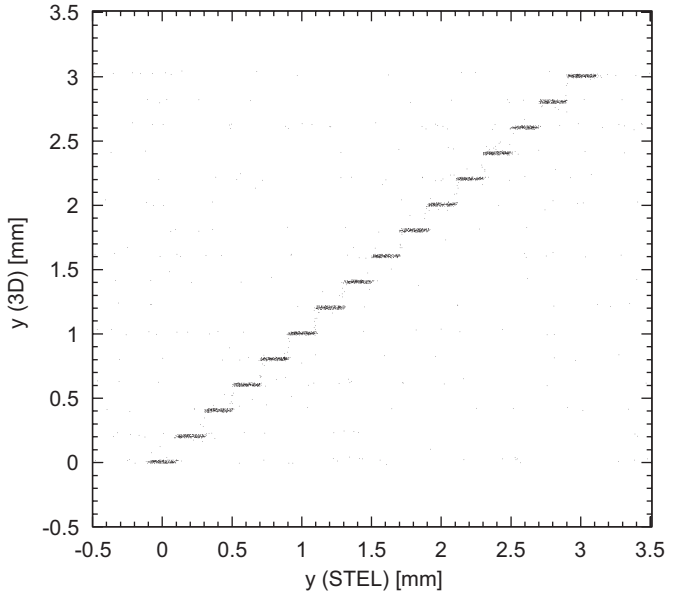

Fig. 1. Correlation between the hit positions y(3D) measured by the 3D detector and the predicted track position y(STEL) showing the spatial resolution comparison between the telescope and 3D detecting elements.

and of the low charge sharing of 3D sensors. This early test used sensors with p^+ signal and n^+ bias electrodes. Modern sensors, including ones matching the ATLAS pixel readout chip, use electron signals, due to the lower electron capture probability in radiation-damaged silicon. We have also taken, in other beam tests, data showing similar stair-step plots using 3D sensors with three-electrode per pixel groups matched to the $50 \times 400\,\mu m^2$ ATLAS pixel size, bump bonded to the ATLAS front-end readout chip [18]. The systems described in this paper use both pixel and separately but simultaneously strip readout electronics use both electron signals and hole signals, and with one exception, use 3D electrode systems. A different system uses a similar name, "stripixel detector" to provide two-coordinate readout from single-sided, planar sensors [19]. In that system, electrodes sending signals to the readouts for the two coordinates are interleaved with a spacing smaller than the size of the charge distribution, after diffusion, from each track.

2. Increased spatial resolution—simultaneous pixel and strip readout

Spatial resolution is generally set by the detecting element pitch, by the spatial characteristics of the ionization along the track, and by the characteristics of the readout electronics. The method used here is to reduce the effective pixel size with readout electronics attached to the bias electrodes, providing a simultaneous readout of n^+ and p^+ electrodes, giving:

1. increased spatial resolution,
2. no significant change in the material budget,
3. no needed change in the in-pixel electronics,
4. with the simplifications of a strip readout, the possibility of a fast trigger.

Use of readout electronics AC coupled to electrodes carrying a DC bias voltage is standard for planar, double-sided strip detectors. The following example uses this double-sided planar technology.

3. Increased spatial resolution in two dimensions using strip readout in one dimension

One method for improving resolution in two dimensions with a single strip-readout in just one dimension is shown schematically in Fig. 2 for planar technology. The dashed lines show the boundaries of four adjacent pixels of the many in a detector chip. The pixel readout side on the bottom surface would have (1) n^+ implants, (2) a p spray implant to trap, in valence bonds, the electrons attracted to the positive oxide interface charge which could short out adjacent n^+ implants, and (3) bump bonds to a readout chip (not shown) below the sensor (the proposed ATLAS upgrade $50 \times 250\,\mu m^2$ pixels would have the aspect ratio of this figure).

Each pixel on the p^+ side, as shown in Fig. 2, has six rectangular pad implants and rectangular metal contacts, three on each long edge. Electrons attracted to the oxide charges on this side tend to isolate these p^+ electrodes from each other. The electrodes in turn are connected to six metal lines, with lines 1, 3, and 5 connected to the pads on one pixel edge and 2, 4, and 6 to pads on the other edge, sub-dividing the pixel into six parts with tracks in each part sending charge to different electrodes. For perpendicular, non-charge sharing tracks, this subdivision doubles the resolution in one dimension and triples it in the other. These lines do not cross the pixel signal lines, as they are on the opposite sensor face from them. An RC connection to isolate the bias voltage from the signal line (the C) and also to prevent the low-impedance supply line from shorting the signal (the R) is also required for both planar

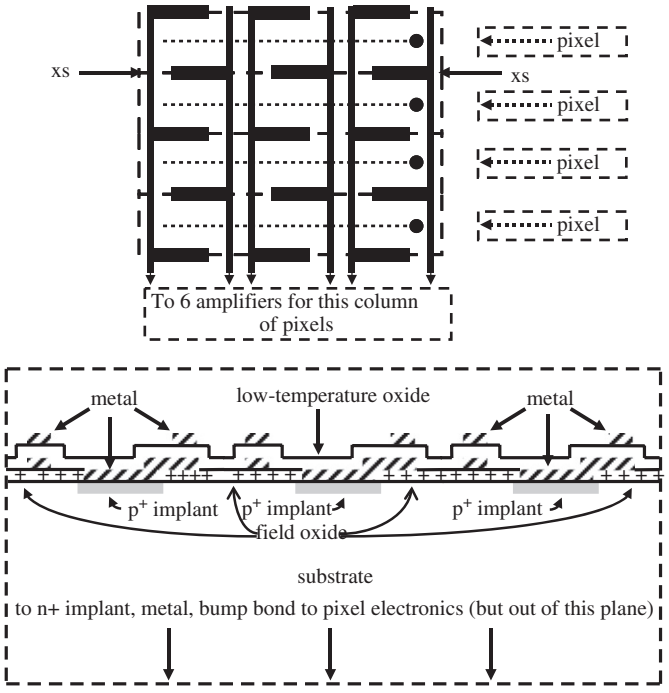

Fig. 2. Top: schematic diagram of a planar-technology, strip-connected pad readout to subdivide each pixel into six sub-parts. Solid lines—metal layers of the strip readout. (On the other side): dotted lines—signal electrodes; solid circles—bump bonds to the pixel readout. If the pixel electrodes are n^+, the strip electrodes will be p^+. Either type of bulk may be used, but p-type bulk will not change type under irradiation. Arrows labeled "XS"–cross-section location. Bottom: cross-section (not to scale) of the section in the top view. Plus signs: location of the positive field-oxide–silicon interface charge. Metal 1 (lower layer, diagonals) contacts the p^+ implants, and joins them via a bus on top of the field oxide with the isolation resistors (not shown here—see Fig. 3) to the bias voltage supply. A dielectric oxide layer, metal 2 (the AC coupled bus) and a scratch mask (a protective layer, not shown) lie above. The pixel implant, metal, and bump bonds on the bottom are out of the plane of the cross-section.

and 3D systems. To avoid both shorting and rate-dependent effects requires:

$$(\text{signal acquisition time}) \ll RC \ll (\text{mean time between signals}). \quad (1)$$

Single hits that share charge with adjacent pads in the same column could cause ambiguities in the column direction, but should usually be resolvable by using the corresponding pixel information. The expected ambiguity rate from multiple hits in the same column of pixels at the LHC is discussed in Section 5.

The direction for the readout strips shown in Fig. 2, in the case of the ATLAS pixel detector, would put the strip readout electronics on the same edge as the pixel control and output circuits, and would allow the other three sides of the complete detector to be placed in close proximity to adjacent detectors. For use in ATLAS, however, this planar addition would actually have less radiation hardness than the present ATLAS planar pixel detectors, which collect electrons, as they would require full depletion and their main signal source would be the motion of the slower and more readily captured holes.

4. Taking signals from 3D bias electrodes

This and the following sections will concentrate, for definiteness, on sensors made with 3D n^+ pixel electrodes and p^+ bias electrodes in a p substrate. The bias electrodes will be isolated at the surfaces by the induced electron sheet, which with our field oxides will have about $2–3 \times 10^{11}$ electrons/cm^2. In the bulk, they will be isolated by the applied reverse bias voltage. As mentioned in Section 3, a p-spray implant is normally used to preserve the isolation at both surfaces of the n^+ electrodes, but now if position information is to be taken from the bias electrodes, that implant would be patterned—made through a mask to keep it away from the p^+ electrodes where it would act as a low-resistance between them.

The horizontal forces from the electrodes will eventually repel the electron sheet and isolate the electrodes, even without an implant, but sometimes only at voltages noticeably larger than otherwise needed for full depletion. The behavior of such a charge sheet was described in Figs. 9 of Ref. [1] and 18 and 19 of Ref. [2] and related text.

In addition, this implant must be large enough to overwhelm the increased oxide charge that results from exposure to radiation. While this increase has been seen to saturate for a fluence of minimum-ionizing particles in the range between 10^{13} and 10^{14} particles/cm^2, the saturation value itself increases with the bias that is applied during the irradiation (see Ref. [20], Fig. 8).

As mentioned in Section 3, a resistor, R, is needed to isolate the signal from the low impedance of the bias supply, and a capacitor, C, is needed to allow the readout electronics to operate near ground potential. In addition to condition (1) in Section 3, transmitting (nearly) the entire signal to the electronics requires:

$$C \gg \text{p-electrodes and connecting bus capacitance.} \quad (2)$$

In the configuration shown in Fig. 3 the resistor (normally made of high-resistivity polycrystalline silicon) and the dielectric are made on the sensor chip. They can also be on a separate RC chip, with the metal bias bus contacting the p electrodes wire-bonded to the RC chip. Fabrication directly on the sensor reduces the total amount of material. It could use the following steps:

1. Deposit ~0.5-μm-thick polycrystalline silicon.
2. Pattern polycrystalline silicon.
3. Pattern metal contact holes in the field oxide.
4. Deposit metal-1 (which will contact one end of the polycrystalline silicon resistors and the electrodes).

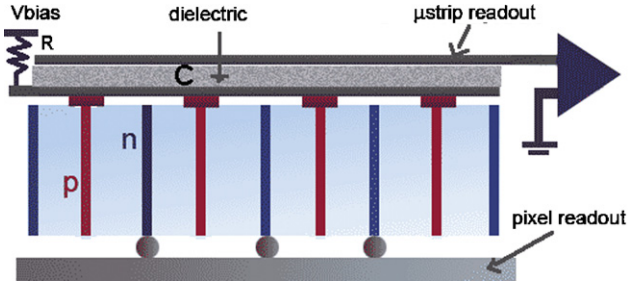

Fig. 3. Sketch of one of the possible dual electrode readout configurations showing a pixel bump-bonded readout at the bottom and bias electrode microstrip readout on top. The resistor, R, keeps the low-impedance bias supply from shorting out the signal, allowing it to be coupled through the capacitance, C, of the dielectric to the readout line. The electrodes extend to the field oxide layers (not shown).

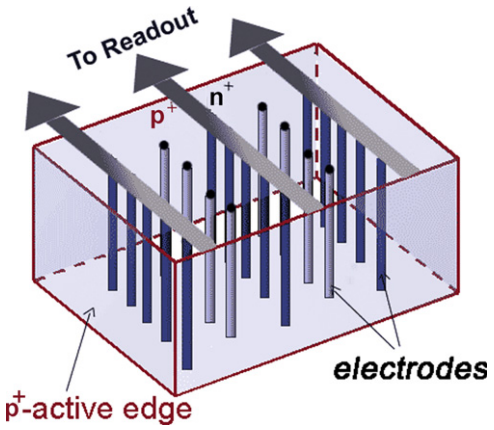

Fig. 4. Three-dimensional schematic view of a same-side strip and pixel readout. The bumps to the pixel readout chip (not shown) are represented by the black dots on the n^+ electrodes. The R and C of Fig. 3 are also needed but, for simplicity, are not shown here.

5. Pattern metal-1.
6. Deposit LTO-1 (low-temperature oxide, layer 1—the dielectric in Fig. 3).
7. Pattern LTO-1 for bias-end polycrystalline silicon contact via.
8. Deposit metal-2 (the top layer in Fig. 3).
9. Pattern metal-2.
10. Deposit LTO-2 (the scratch mask, for general protection).
11. Pattern LTO-2 (wire-bond contact vias for metal-2).

It could also be possible to replace metal 1 with a heavily doped polycrystalline silicon layer and the LTO of step 6 with a thermal oxide. (However oxidizing the boron-doped polycrystalline silicon that would join the p^+ electrodes produces a glass that is difficult to etch.) An alternative configuration, shown in Fig. 4, would have both readouts on the same side. For the ATLAS pixel configuration, this readout, while still on the same side as the pixel readout, can have the output rotated 90° parallel to the column direction as shown in Fig. 5 without crossing any other metal lines.

Fig. 5 shows the locations of the p^+ implants that are needed to keep electrons attracted to the positive oxide interface charge from shorting out the n^+ signal electrodes. When the p^+ bias electrodes, from which signals are also to be taken, penetrate to the same surface, an unmasked p-spray would short them out, hence the need for the opposite-side mask step. If the p^+ bias electrodes did not penetrate all of the way to that side—just moderately close—an unmasked p-spray would not short them. This however, would have larger electric fields at the ends of the

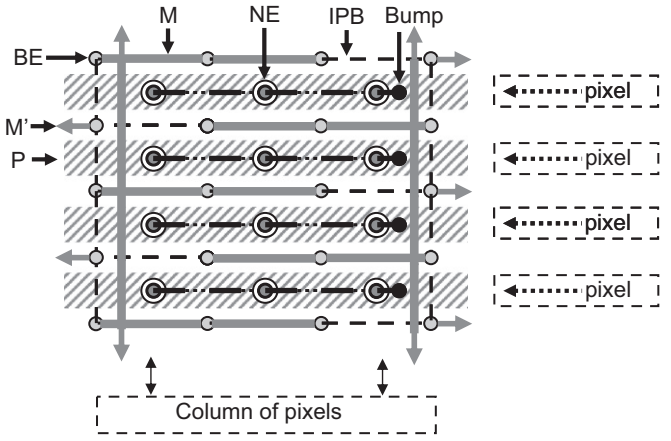

Fig. 5. Schematic diagram of a strip readout on the same side as the pixel readout, to subdivide each pixel into sub-parts. (BE) gray circles—p^+ bias electrodes, (M) connecting gray lines—strip readout, (M′) gray arrows—strip readout lines to adjacent pixels, (P) p+ implants (diagonal shading, implant is on both surfaces), (NE) gray circles with black borders—n^+ pixel signal electrodes, surrounding circles—limit of p+ implant region, (IPB) dashed rectangles—pixel borders (not visible when under metal), (Bump) black circles—bump bonds, dash-dot lines—metal connecting bumps to n^+ electrodes.

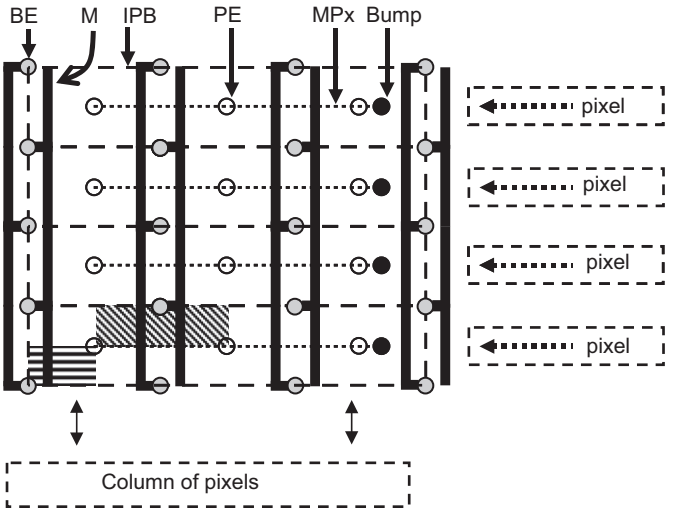

Fig. 6. Schematic diagram of a strip readout on the opposite side of a pixel readout to subdivide each pixel into 6 sub-parts (2 are shaded). (BE) bias electrodes, (M) strip readout, (IPB) dashed lines—inter-pixel boundaries, and, on the other side, (PE) open circles—pixel signal electrodes, (MPx) dotted lines—connecting metal, (Bump) bump bonds. The p^+ implants, shown in Fig. 5 are also used here on both sides, but not explicitly shown to keep the diagram uncluttered.

electrodes and would require, across the entire wafer, a very uniform etch rate and a very precise known rate or some method of on-line monitoring of the etch distance. For example, 240 μm electrodes in a 250 μm substrate would have a 10 μm gap that would vary by 50% for a 2% change in etch rate. With the present method, etching simply ends at the field-oxide, which acts as an etch-stop.

Finally Fig. 6 shows an arrangement, now needing both sides to avoid high-capacitance metal-over-metal crossings, in which each pixel is sub-divided into four central and four half-width border regions. One central and one border region are shown with diagonal and horizontal line fill. They can be distinguished by which bias electrode carries the hole signal, and for the two halves of the border region, by which pixel has the electron signal. For the present ATLAS pixel readout with 18 columns of 400-μm-long pixels, arrayed in 180 50-μm-wide rows, the central strip pitch can be (400 μm)/(the number of 3D signal electrodes per pixel). Sensors made so far have 2, 3, and 4 electrodes per pixel. Fig. 6, for example shows 3 per pixel, surrounded by 8 bias electrodes, which are shared with neighboring pixels. The proposed readout for the upgraded pixel detector would still have 50-μm-wide pixels, but they would be 250-μm-long. They could have 2 or 3 electrodes per pixel. The required input pitch for a strip-readout VLSI chip then would be the pixel length divided by two times the number of signal electrodes per pixel −50–100 μm now and either 62.5 or 41.66 μm for the new readout chip. All designs would provide 25 μm wide sub-pixels, with the possibility of also recognizing hits close to the middle that contribute to signals on both sets of bias electrodes.

With modern electronics, the channel widths for the strip readout chips should be small enough to handle this pitch, even with the use of the enclosed gates and guard rings of radiation-hard technology [21]. A 50 μm input pitch is absolutely standard for strip detector amplifiers—the first-ever VLSI silicon-strip readout chip, fabricated in a university lab in early 1984, using 5 μm technology, actually had a fan-in from its 50 μm wire-bond pad pitch (staggered into 4 rows) to the 35 μm circuit pitch [22].

5. Multiple-hit ambiguities

Both parallel and orthogonal readouts are subject to ambiguity. The parallel readout is subject to ambiguity when adjacent strips have signals corresponding to two hit pixels both of which are between the strips. The orthogonal readout is ambiguous whenever two or more strips crossing the same set of pixels have hits. The half-length edge regions of Fig. 6 are subject to ambiguity if a second hit occurs in the adjacent column of pixels.

An estimate for the probability of ambiguous results can be made using Figs. 3-39 and 3-40 of the ATLAS Inner Detector Technical Design Report [23], which give the occupancies per readout column for the then design pixel length of 300 μm. Multiplying by 4/3, at a luminosity of $10^{34}\,cm^{-2}\,s^{-1}$, in the B-layer, in the core of a B jet, the probabilities of 2, 3, and 4 triggered pixel cells are 2.2%, 0.34%, and 0.12%. Some of these double-cell events might be resolved by comparing pulse heights. In addition, for the odd–even hit bias electrode schemes of Figs. 2, 5 and 6 that reduce the 50 μm width to 25 μm, half of the 2.2% of events will be in the same part of their pixels, leaving 1.1% to be possibly resolved by differing pulse heights.

6. Separate or combined strip and pixel readout chips

Initial tests will most easily be done with the pixel readout chip underneath and bump bonded to the sensor with a strip readout on top. This would require only extra metal and low-temperature oxide layers on top of the sensor, with wire bonds extending to a separate RC chip and from there to a separate silicon-strip amplifier. The next step would be to fabricate the RC elements directly on the sensor as mentioned in Section 4. The most compact, with the least material, would still have the RC elements including bias voltage distribution on top, with a wire-bond connection to the bias supply. The topside signal-carrying strips would then be connected with an extra row of 3D low-resistance polycrystalline silicon electrodes to an extra row of bump-pads on the bottom. These would lead to the strip readout and would be included in the pixel chip. Those top-to-bottom connecting electrodes might be isolated from the substrate with a lining of oxide (requiring extra fabrication steps, which are never easy and may lower the yield) or since their DC voltage is now

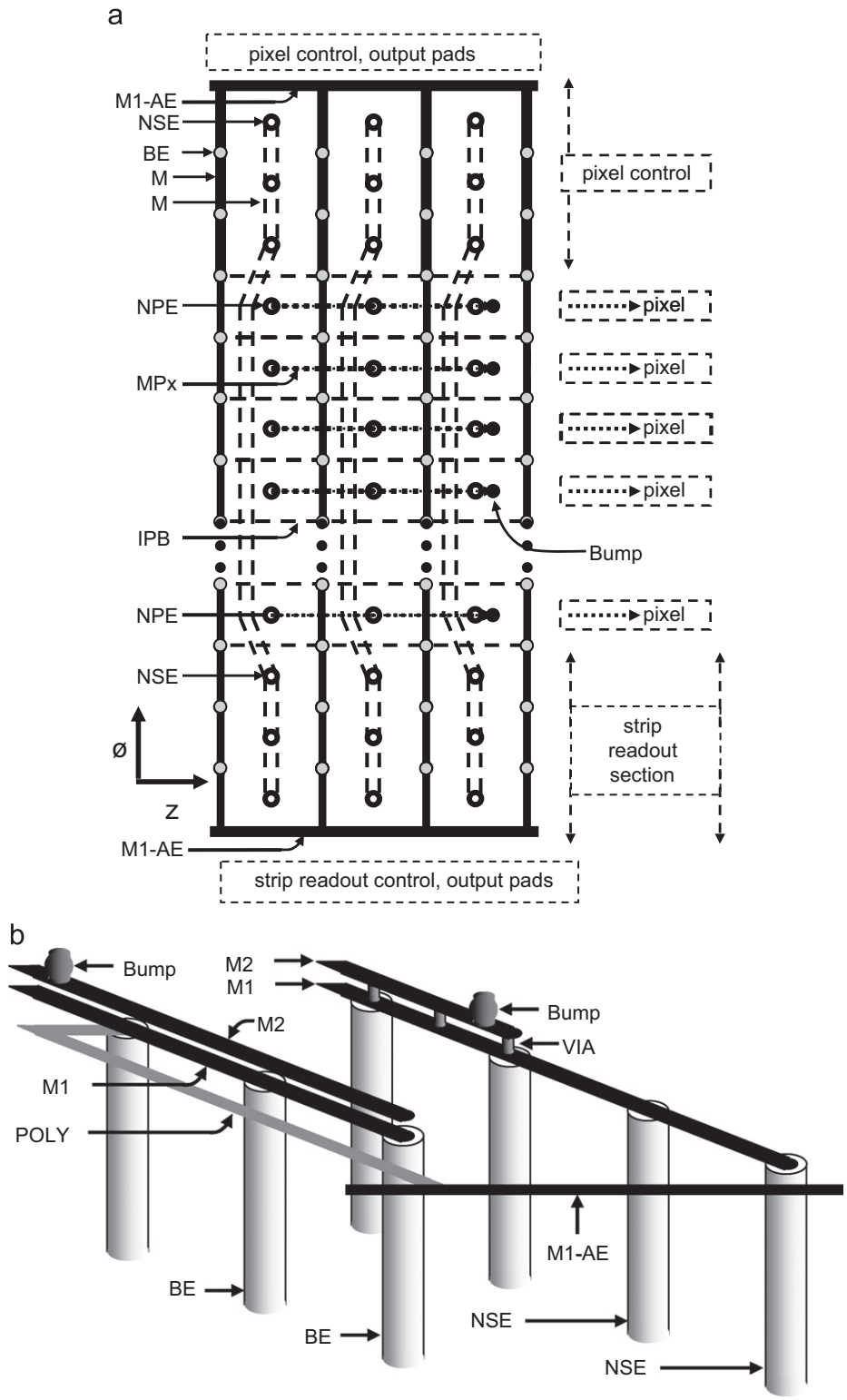

Fig. 7. (a) View of one column of pixels with the active-edge sensor extending under the pixel readout control and strip electronics, providing full-area sensitivity with the pixel readout in the center and the strip readout up to start of the wire-bond pads. (For clarity, the number of electrodes is limited in this figure. The actual number of rows of n-p electrode pairs would be many tens in the pixel-control and strip-readout sections, and up to several hundreds in the pixel sensor section.) This view shows conductors on the side away from the readout electronics and two items on the electronics side: the bump-bond and the conductor connecting it to the 3D n^+ pixel electrodes. (M1-AE)-metal layer 1 along active-edge, (NSE)-n^+ strip section electrode, (BE)-bias electrode, (M)-metal lines, (MPx)-level 1 metal line (on other side), (NPE)-n^+ pixel electrode, (IPB).-inter-pixel boundary (not visible where it is under metal) (b) View of part of one column of bias and strip electrodes (the lower-left corner of figure 7a), showing just the conductors on the readout electronics (bump) side of the sensor near the active-edge of the strip-readout section. (M1-AE)-metal layer 1 along active-edge, (NSE)-n^+ strip electrode, (BE)-bias electrode, (M1)-level 1 metal line, (M2)-level 2 metal line, (VIA) M1-M2 connection, (POLY)-high resistance polycrystalline resistive connection to bias electrodes from the active-edge metal. The metal lines M1 and M2 would actually be wider than the diameters of the electrodes BE and NSE, particularly at the electrodes, but are drawn narrower so they and the connecting vias can be distinguished from each other. If it is necessary to have wire-bond pads along only one edge, the pixel control and strip readout electronics could be on only one side, but then the small strip signals would need to be protected from larger digital signals.

close to that of the signal electrodes, a lower-capacitance back-biased junction similar to those of the signal electrodes. This method does have a small, but non-zero, probability of wrong-sign pulses from tracks penetrating the immediately surrounding substrate. Finally, in the next section this method will be extended to address two of the major problems facing the inner layers of vertex detectors at the planned upgraded LHC—reducing insensitive material and improving the z-resolution so tracks from closely spaced events will be assigned to the correct vertices.

7. Full-area, high-z resolution systems

The silicon vertex detectors at the LHC will not have sufficient resolution to separate events in the same beam crossing based on their vertex position in the transverse plane, only the z-coordinate, parallel to the beam direction can be used. The need for sufficient pixel area to contain the electronics and for resolution in the transverse plane, limits how small the pixels can be in the z-direction. After the planned intensity increase, separating tracks from different vertices will be difficult. Fig. 6, combined with the readout suggestions of Section 6 shows one method by which that can be done. Fig. 7a shows a design that provides track detection with high-resolution z-sensitivity in the regions under the strip readout and pixel control sections of a common readout chip as well as in the pixel detection region. The sensor and 3D pixel electrode array is extended to those two regions with metal strips linking both n and p electrodes, with the n-strip skipping the electrodes in the pixel section, jogging over a bit, as shown in Fig. 7a, to minimize the capacitance to the n-pixel electrodes. The track location of the bias-electrode signals can be assigned to the pixel—control+strip—readout section or the pixel section, depending on the presence or not of a signal on a matching n-channel. The need for full-depletion operation and relatively low-bias voltage needed to reach it, allows the signals to be brought through the bulk to the electronics readout side by the electrodes themselves.

Fig. 7b shows some of the details. The bias voltage comes from a metal line in contact with the doped silicon at the active edge. Individual bias-electrode signal channels are connected to it via a high-resistance polycrystalline silicon conductor, so the fast signal does not see the ac ground of the bias supply, but goes through the capacitor formed by a layer of deposited oxide and the M1–M2 metal layers to a near-ground voltage amplifier input. (Unlike those in Section 4, these resistors contact metal 1 at both ends.) The length of that capacitor should be long enough so the M1–M2 capacitor is much larger than the capacitance of the electrodes attached to M1. The voltage of the line connecting the n^+ electrodes is already close to ground, but the path for signals is shown going from M1 to M2 metal by way of vias, to keep the M2-readout chip input separation equal for both types of signals. This may not be necessary for some bump technologies.

The bias electrode bump active edge distance is shown as being larger than the n^+ bump active edge distance. This allows the full channel width of the strip amplifier to be devoted to an extra stage for the bias-signal input. The extra inverter can be designed to handle the higher input capacitance of that signal, and makes a common polarity for all outputs. This could allow time-over-threshold pulse-height readout for the strips as well as for the pixels. Such pulse height information could improve the z-resolution for angled tracks that cross more than one channel in the end regions of the detector, and could be useful as mentioned in Section 5, in resolving multiple-hit ambiguities. Separate from this, these column busses provide places where circuitry could also be added for a fast trigger.

Fabrication steps will differ somewhat from those of Section 4 due to the need for double metal and capacitors on the circuit side rather than the opposite one, and the possible use of vias to connect the two metal layers.

8. Conclusions

Methods are described using a combination of standard pixel electronics with an added strip readout, could also provide a fast trigger with a similar improvement in spatial resolution.

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