CMB Test Board

CAN Bus Access

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Operation Modes

Two operation modes are implemented on the Test Board:

Test Mode (Jumper J6 closed)

In Test Mode the CAN Bus access is disabled.

LED's **D12-D19** are controlled by switch block **SW2** and LED's **D20-D23** are controlled by the first four switches of switch block **SW1**.

CAN Mode (Jumper J6 open)

In CAN Mode the Test Board is completely controlled via the CAN Bus.

The following functions are implemented:

- Control of LED's D12-D23
- Programming of DAC A and DAC B
- Reading of ADC Control Registers
- Setting of ADC Control Registers
- ADC Reset
- Reading of ADC measurement values for 16 input channels
- Enabling the Board to periodically send the ADC measurement values
- Reading of interface status information.

Necessary information about the CAN bus access to the Test Board are given in the following chapters.

CAN Higher Level Protocol

Devices connected to a CAN bus have to follow a so called CAN Higher Level Protocol, which includes the Baud rate and the Identifier definition. For the Test Board the following parameters are fixed by firmware:

- Baud Rate: 125 kHz
- Identifier: 11 Bit Standard: ID10..ID0
- Identifier Definition: **ID = $500 + 2 * BAD**

The Board Address **BAD** can be selected by means of a six fold switch **SW1**. A change on that switch becomes effective only after power-on reset.

Six functions are defined:

- Function F1: Set LED's
- Function F2: Set DAC's
- Function F3: Write ADC Control Registers
- Function F4: Read ADC Control Registers
- Function F5: Read ADC Measurement
- Function F6: Read Status

The Function Number **FN** and the number **SN** of it's sub-function are transmitted by the first data byte of the message according to the equation

DB = FN * $10 + SN

All messages are data messages (RTR Bit = 0) with at least one data byte (argument).

The controller responds to the requests by sending a data message with an identifier, which is incremented by one.

Additionally the controller sends unrequested messages with Function F15, if it is enabled for periodic ADC data transmission.

In the following chapter the functions and the corresponding response messages are described in more detail.

CAN Bus Functions

(All numbers are hexadecimal)

Function F1: Set LED's

Identifier	DLC	Byte 1	Byte 2	Byte 3	Function
ID	3	11	LVL	LVH	Set LED's

LVL: Bit n (0<=n<=7) switches LED D12+n
LVH: Bit n (0<=n<=3) switches LED D20+n

Function F1 generates the following response:

F1(1) Set LED's:

Identifier	DLC	Byte 1
ID+1	1	11

Function F2: Set DAC's

Identifier	DLC	Byte 1	Byte 2	Function
ID	2	21	**DATA**	Set DAC A
ID	2	22	**DATA**	Set DAC B
ID	2	23	**DATA**	Set DAC A and DAC B

DATA: Data Byte, to be written to the DAC

Function **F2** generates the following response:

F2(1) Set DAC A:

Identifier	DLC	Byte 1
ID+1	1	21

F2(2) Set DAC B:

Identifier	DLC	Byte 1
ID+1	1	22

F2(3) Set DAC A and DAC B:

Identifier	DLC	Byte 1
ID+1	1	23

Function F3: Write ADC Control Registers

Identifier	DLC	Byte 1	Byte 2	Byte 3	Function
ID	3	31	REGL	REGH	Write Mode Register
ID	3	32	REGL	REGH	Write Configuration Register
ID	3	33	REGL	REGH	Write Offset Register
ID	3	34	REGL	REGH	Write Full Scale Register
ID	2	35	TINT		Write Time Interval (sec)
ID	1	36			Reset ADC

REGL: Least significant Byte, to be written to the Register
REGH: Most significant Byte, to be written to the Register
TINT: Time Interval for Periodic ADC Data Transmission (0 <= TINT <= 255)
TINT = 0: Periodic ADC Data Transmission is disabled
ADC Reset: The ADC is reset and the ADC Registers are set to the default values.

Function **F3** generates the following response:

F3(1) Write ADC Mode Register:

Identifier	DLC	Byte 1
ID+1	1	31

F3(2) Write ADC Configuration Register:

Identifier	DLC	Byte 1
ID+1	1	32

F3(3) Write ADC Offset Register:

Identifier	DLC	Byte 1
ID+1	1	33

F3(4) Write ADC Full Scale Register:

Identifier	DLC	Byte 1
ID+1	1	34

F3(5) Write ADC Time Interval:

Identifier	DLC	Byte 1
ID+1	1	35

F3(6) Reset ADC:

Identifier	DLC	Byte 1
ID+1	1	36

Function F4: Read ADC Control Registers

Identifier	DLC	Byte 1	Function
ID	1	41	Read Status Register
ID	1	42	Read Mode Register
ID	1	43	Read Configuration Register
ID	1	44	Read ID Register
ID	1	45	Read Offset Register
ID	1	46	Read Full Scale Register
ID	1	47	Read Time Interval

Function **F4** generates the following response:

F4(1) Read Status Register:

Identifier	DLC	Byte 1	Byte 2
ID+1	2	41	STAT

STAT: ADC Status Byte (see ADC Data Sheet)

F4(2) Read Mode Register:

Identifier	DLC	Byte 1	Byte 2	Byte 3
ID+1	3	42	MODL	MODH

MODL: LSByte of ADC Mode Register (see ADC Data Sheet)
MODH:MSByte of ADC Mode Register (see ADC Data Sheet)

F4(3) Read Configuration Register:

Identifier	DLC	Byte 1	Byte 2	Byte 3
ID+1	3	43	CONL	CONH

CONL: LS-Byte of ADC Configuration Register (see ADC Data Sheet)
CONH: MS-Byte of ADC Configuration Register (see ADC Data Sheet)

F4(4) Read Identification Register:

Identifier	DLC	Byte 1	Byte 2
ID+1	2	44	ID

ID: ADC Identification Byte (see ADC Data Sheet)

F4(5) Read Offset Register:

Identifier	DLC	Byte 1	Byte 2	Byte 3
ID+1	3	45	OFSL	OFSH

OFSL: LS-Byte of ADC Offset Register (see ADC Data Sheet)
OFSH: MS-Byte of ADC Offset Register (see ADC Data Sheet)

F4(6) Read Full Scale Register:

Identifier	DLC	Byte 1	Byte 2	Byte 3
ID+1	3	46	FSL	FSH

FSL: LS-Byte of ADC Full Scale Register (see ADC Data Sheet)
FSH: MS-Byte of ADC Full Scale Register (see ADC Data Sheet)

F4(7) Read Time Interval:

Identifier	DLC	Byte 1	Byte 2
ID+1	2	47	INT

INT: Time Interval (sec) for periodic ADC Data Transmission

Function F5: Read ADC Data

Identifier	DLC	Byte 1	Function
ID	1	51	Read Channel 0 & 1
ID	1	52	Read Channel 2 & 3
ID	1	53	Read Channel 4 & 5
ID	1	54	Read Channel 6 & 7
ID	1	55	Read Channel 8 & 9
ID	1	56	Read Channel 10 & 11
ID	1	57	Read Channel 12 & 13
ID	1	58	Read Channel 14 & 15

Function **F5** generates the following response:

F5(1) Read Channel 0 & 1:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	51	ST0	DL0	DH0	ST1	DL1	DH1

F5(2) Read Channel 2 & 3:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	52	ST2	DL2	DH2	ST3	DL3	DH3

F5(3) Read Channel 4 & 5:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	53	ST4	DL4	DH4	ST5	DL5	DH5

F5(4) Read Channel 6 & 7:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	54	ST6	DL6	DH6	ST7	DL7	DH7

F5(5) Read Channel 8 & 9:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	55	ST8	DL8	DH8	ST9	DL9	DH9

F5(6) Read Channel 10 & 11:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	56	ST10	DL10	DH10	ST11	DL11	DH11

F5(7) Read Channel 12 & 13:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	57	ST12	DL12	DH12	ST13	DL13	DH13

F5(8) Read Channel 14 & 15:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	58	ST14	DL14	DH14	ST15	DL15	DH15

STn: Status Byte of Channel n
Bits 0..3: Channel Nr.
Bit 4: 0: Setting of ADC Mode Register was successful
1: Setting of ADC Mode Register was not successful
Bit 5: 0: Setting of ADC Configuration Register was successful
1: Setting of ADC Configuration Register was not successful
DLn: LS-Byte of Data of Channel n
DHn: MS-Byte of Data of Channel n

Function F6: Read Status

Identifier	DLC	Byte 1	Function
ID	1	61	Read CAN Error Bytes
ID	1	62	Read Firmware Release Nr.

Function **F6** generates the following response:

F6(1) Read CAN Error Bytes:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4
ID+1	4	61	CEB	TEC	REC

CEB:
C0: Error Warning Bit (C1 or C2 are set)
C1: Receiver Warning Bit (95 < REC < 128)
C2: Transmitter Warning Bit (95 < TEC < 128)
C3: Receiver Bus Passive Bit (127 < REC)
C4: Transmitter Bus Passive Bit (127 < TEC)
C5: Transmitter Bus Off Bit (255 < TEC)
C6: Receiver Buffer 1 Overflow Bit
C7: Receiver Buffer 0 Overflow Bit
TEC: Transmitter Error Counter
REC: Receiver Error Counter

For more details of the CAN error handling please consult the CAN Bus Specification manual (CAN Specification, Version 2.0, Robert Bosch GmbH, 1991).

F6(2) Read Firmware Release Number

Identifier	DLC	Byte 1	Byte 2	Byte 3
ID+1	3	62	VNH	VNL

VNH: MS-Byte of Version Number
VNL: LS-Byte of Version Number

Unrequested Messages

The controller can be enabled to periodically send the ADC measurement data by setting the Time Interval T [sec] to a value between 1 and 255 by means of Function F3(5). Every T seconds then the controller transmits 8 frames in the following format:

Channel 0 & 1:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F1	ST0	DL0	DH0	ST1	DL1	DH1

Channel 2 & 3:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F2	ST2	DL2	DH2	ST3	DL3	DH3

Channel 4 & 5:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F3	ST4	DL4	DH4	ST5	DL5	DH5

Channel 6 & 7:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F4	ST6	DL6	DH6	ST7	DL7	DH7

Channel 8 & 9:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F5	ST8	DL8	DH8	ST9	DL9	DH9

Channel 10 & 11:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F6	ST10	DL10	DH10	ST11	DL11	DH11

Channel 12 & 13:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F7	ST12	DL12	DH12	ST13	DL13	DH13

Channel 14 & 15:

Identifier	DLC	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
ID+1	7	F8	ST14	DL14	DH14	ST15	DL15	DH15

STn: Status Byte of Channel n
Bits 0..3: Channel Nr.
Bit 4: 0: Setting of ADC Mode Register was successful
1: Setting of ADC Mode Register was not successful
Bit 5: 0: Setting of ADC Configuration Register was successful
1: Setting of ADC Configuration Register was not successful
DLn: LS-Byte of Data of Channel n
DHn: MS-Byte of Data of Channel n

The unrequested messages are protected by a time-out. In case of bus errors or permanent lost bus arbitration it gives up after one second and tries again, when the time interval has been passed.